Signal Integrity

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1. Introduction

High speed Printed Circuit Board design is a complex matter. This white paper will discuss the most relevant phenomena that should be addressed when designing reliable systems. Reliability can only be achieved by insuring the integrity of the signals running from component to component on the PCB. Hence the term “Signal integrity”. It is the intention of this white paper to provide an overview of all the matters that affect high speed designs.

Without the appropriate attention for signal integrity, the functioning and reliability of the board cannot be guaranteed. As a result the PCB that is produced most surely will not work which results in a redesign causing additional cost and delay. The traditional way of debugging hardware designs by patching boards is not possible at high frequencies.

What is Signal Integrity?

The quality of an electrical signal or pulse on the interconnect track of a PCB or component. Electronic signals, particularly high speed ones will deteriorate, distort or oscillate if the designer has not made allowances for impedance matching and signal transmission effects.

This means, that interconnects have to be represented by a transmission line models in order to simulate the circuits to predict correct functioning before any hardware is produced. Additional effects that substantially determine the signal integrity of a signal are; timing (jitter), crosstalk and ground bounce.

Why is Signal Integrity becoming more and more important?

Through the years the speed (rise and fall times) of electrical signals in digital systems has been increased with factors. Where in 1985 PCs where operating at a frequency of 4MHz, today’s PCs operate at 4GHz with rise and fall time smaller than 150ps.

Likewise the electrical signal levels have been decreased to make these speeds possible. Because the signal levels have been decreased, the influence of noise has been increased. In 1985 5V voltage levels were used, today signal levels have dropped to as low as 300mV.
2. Transmission lines

An ideal transmission line, with a resistive termination equal to the characteristic impedance, will show the same signal amplitude on both ends of the transmission line. In real life however, these systems are never ideal. A lot of phenomena endanger the transfer characteristics. These phenomena may lead to; reflections, attenuation, crosstalk, jitter and ground & rail bounce. These phenomena will be addressed in detail later.

When the propagation time is equal to or smaller than 1/6th of the rise- and fall time wavelength, an interconnection between two ICs should be treated as a transmission line. The propagation time can be calculated with the following formula;

\[ c' = \frac{c}{\sqrt{\varepsilon_r}} \]

FR4 has a \( \varepsilon_r \approx 4.5 \), \( c = 299.792.458 \text{ m/s} \) => \( c' \approx 140.000.000 \text{ m/s} \)

Example: Given a clock signal of 100MHz (period time = 10ns) and a rise and fall time of 1ns an interconnection length greater than 2.3cm should be considered a transmission line.

An ideal transmission line only consists of series inductances and shunt capacitances and does not have any loss. With an ideal transmission line there will be no attenuation and no frequency dependencies. With a correct resistive terminated transmission line, whatever signal is applied at the output will occur at the input after the propagation time of the transmission line. The impedance of the transmission line can be calculated with the following formula:

\[ Z_o = \sqrt{\frac{L_i}{C_i}} \]

![Figure 1: Ideal transmission line representation](image)

In practice there are many effects that cause the transmission lines not to be ideal. The effects are series resistance due to conductor resistance and parallel shunt conductance caused by the dielectric. This transmission line is also called a “lossy” transmission line. The transmission line can be represented as shown in the figure below and the lossy impedance can be calculated with the following formula:

\[ Z_o = \sqrt{\frac{L_i + R_i}{C_i + G_i}} \]

![Figure 2: Lossy transmission line representation](image)

The resistive (R) and conductive (G) components in the formula are not fixed values but are frequency dependent. Because the resistance (R) and conductance (G) are frequency dependent components they become more important with increasing signal frequencies.
3. Reflection

Reflections are caused by discontinuities in the interconnect track impedance and will reflect part of the signal back to the source. The impedance of the ideal transmission line is:

\[ Z_0 = \sqrt{\frac{L}{C}} \]

\( L \) and \( C \) are the inductance and capacitance per unit of length, every disturbance of the capacitance or the inductance causes a reflection. The amplitude on the reflection depends on the value of disturbance and the rise time of the signal. In Figure 3 an overview is given of the different terminations and impedance disturbances and their effect on the reflected signal.

In an ideal design, impedance disturbances are avoided and transmission line termination is identical to the line impedance. In real life designs however, impedance disturbances cannot be avoided and will distort the transmitted signal. The main goal is to keep the disturbances within acceptable levels during the design phase.

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**Figure 3: Transmission line termination and discontinuities**

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**Figure 4: Example of interconnect disturbance sources**
To be able to guarantee the correct interpretation of the signal on the receiver end, the different sources of disturbance need to be known and it is essential to be able to quantize the effect of the disturbance. Different sources of disturbance are:

- through hole vias & ICT measure points (pad or via);
- stubs;
- bends in the trace;
- return path disturbances;
- SMD pads;
- connectors;
- impedance mismatches.

3.1 Through hole vias

In most designs each trace contains one or more vias to switch between signal layers and to enable routing (fan out) of large pin count BGA packages. There are three types of vias; blind vias, buried vias and through hole vias. Blind and buried vias have a good high frequency performance but are very costly. Therefore, through hole vias are still widely used in high speed designs.

To be able to use the through hole vias in high speed traces a lot of care has to be given to the design of the via. A well dimensioned via will keep the signal disturbance to acceptable levels. There are two main effects that are involved with vias to care about in high speed designs:

- via impedance;
- via stub.

A via has an inductance and capacitance that determine the impedance. When the impedance of the via is identical to that of the transmission line there will be no signal disturbance. For a through hole via the impedance can be calculated. By varying the clearance hole diameter in the power and ground planes, the inductance can be tuned to the line impedance.

3.2 Stubs

Stubs are non-terminated lines connected to a trace between transmitter and receiver. Stubs will act as a shunt capacitance on the transmission line and look...
like a short circuit for a specific frequency. The longer the stub, the lower the frequency at which it will act as a short circuit. Stubs can be either a trace on a circuit board or a via stub.

3.2.1 Via stubs
When a through hole via is used to switch layers in a PCB, the length of the via that is not used for the interconnection will act as a shunt capacitance.

![Diagram of via stubs](image)

The stub length depends on which layer the traces are routed on (see above). For high speed signals there are preferably no stubs and only the outer layers will be used for routing.

3.2.2 Trace stubs
Special care has to be given to stubs on traces as they react like a shunt capacitance. A stub can easily exist when a transmission line contains pull-up or termination resistors.

\[
C_{stub} \approx 0.00885 * \varepsilon_r * W * \frac{l}{d} \quad [pF]
\]

With dimension \((W, l\) and \(d\)) in mm

When \(l = \frac{\lambda}{4}\), the stub will be short circuit

\[
\lambda = \frac{c}{f} = 0.14 \frac{\text{meter}}{\text{GHz}}
\]

A stub will act as a short circuit when the length is equal to a quarter of the wavelength.

*Example:* Given a 10GHz sine-wave signal a stub of \(L = 0.014m / 4 = 0.0035\) meter = 3.5mm will act as a short circuit on the transmission line.
3.3 Trace bends

Trance bends are not transparent to a high-frequency electrical signal. Any trance bend will result in a shunt capacitance on the transmission line.

![Diagram of trace bends](image)

**Figure 7: Trace bends**

With a 90 degree bend the effective trace length increases in the corner and will result in a shunt capacitance on the line.

\[
C_{90°} \approx \frac{2.4 \times W \times \sqrt{\varepsilon_r}}{Z_0} \quad [pF] \quad \text{with } W \text{ in mm}
\]

*Example;* \( W=250\mu m \) (10mil), \( Z_0=50\Omega \), and \( \varepsilon_r=4.5 \); \( C_{90°} \approx 0.025pF \)

Rounding of the corner is relatively difficult for CAD tools, thus the corner can be chamfered to reduce the shunt capacitance.

45 degree bends are better than the 90 degree bends but they are not perfect.

\[
C_{45°} \approx \frac{0.49 \times W \times \sqrt{\varepsilon_r}}{Z_0} \quad [pF] \quad \text{with } W \text{ in mm}
\]

*Example;* \( W=250\mu m \) (10mil), \( Z_0=50\Omega \), and \( \varepsilon_r=4.5 \); \( C_{45°} \approx 0.005pF \)

Curved bends are the best but still not perfect. Rule of thumb is to use a minimum radius of two times the width.

3.4 HF Current return path

Every transmission line requires a current return path parallel to the transmission line. Apart from forming a source for emission, any disturbance in the return path will also result in an impedance mismatch. The disturbance in the current return path will act as a series inductance in the transmission path.
For high speed traces it is therefore important that there are no interruptions underneath the signal trace in the power or ground plane to which the signal is referenced. Special care should be given to high speed traces that switch from one layer to another. The plane to which the high speed signal is referenced will also change because of switching layers. There should be a coupling between the two reference planes as close to the position of the signal switches layers as possible.

In case the reference plane changes from power to ground or vice versa, a capacitor should be placed close to the via which is used to switch signal layers. The capacitor creates a high-frequency coupling between the planes to guide the return current.

**3.5 Pad capacitance**

With high frequencies the capacitance of a pad will cause a shunt capacitive disturbance on the transmission line impedance. The capacitance depends on the size of the pad, the relative dielectric constant, and the distance to the return (ground) plane.

In many high speed serial links (such as PCI-Express and XAUI) DC blocking capacitors are used to decouple the common mode voltage of the transmitter and receiver. The pads of the DC blocking capacitors will give an impedance disturbance on the transmission lines.
A way to reduce the capacitance is to use the smallest components that are allowed to be used and make cut-outs in the reference plane underneath the pads.

\[ C_{pad} \approx \frac{0.00885 \cdot \varepsilon \cdot A \cdot B}{d} \text{ [pF]} \]

A = pad length in [mm]
B = pad width in [mm]
d = distance between pad and reference layer [mm]

3.6 Connectors

In general a connector will act as a series inductance in the transmission line, the connector can be represented as an inductor with two capacitors. For high frequencies, special impedance matched connectors are available so that they cause minimum disturbance.

![Connector representation](image)

When the inductance of the connector is greater than the capacitance on both ends, the disturbance on the transmission line becomes inductive.

3.7 Impedance mismatch

Impedance mismatch between two transmission lines or between transmission line and termination impedance causes reflections. Impedance mismatch between two transmission lines can be the difference in impedance between layers or the difference between the trace impedance and load impedance.

![Impedance mismatch](image)

Due to PCB process variations, the impedance of the traces can vary as much as 10% of the calculated value.
4. Attenuation

When a signal output and an input are connected through a transmission line, the voltage at the receiver input will be less than the voltage at the transmitter output. This is called attenuation. There is always a margin between the delivered output voltage and the required input voltage. The sum of all attenuation sources should never exceed this margin. This has to be calculated for all transmission lines.

Sources of attenuation are:
- Termination loss
- Conductor loss
- DC loss (Copper loss)
- AC loss (Skin effect)
- Dielectric (εr) loss

The above figure is an example of the conductor and dielectric loss of a differential signal on a default FR4 PCB. As can be seen, the attenuation is rapidly increasing for high frequencies. Every 6dB attenuation will halve the amplitude of the signal thus 12dB will be 25%, 18dB is 12.5%, etc. The frequency dependent loss will result in Inter-symbol interference.

4.1 Termination loss

Adding a parallel and/or series termination to a signal, results in a resistive divider.

\[
\frac{U_i}{U_o} = \frac{R_{pt}}{R_i + R_{ser} + R_c + R_{pt}}
\]

With Uo is the open output voltage.
The resistors in the chain are:
- $R_i$: internal resistance of the output buffer
- $R_{st}$: series termination to prevent reflections to bounce to and fro
- $R_c$: copper resistance of the trace
- $P_{pt}$: parallel termination for characteristic termination of the transmission line

4.2 Conductor losses

Due to the resistance of a conductor (in most cases copper) a signal travelling through the conductor will experience loss. The conductor loss can be divided into two parts; DC loss and AC loss. Both DC and AC loss are due to the same conductor resistance. AC currents through a conductor cause effects which increase the conductor resistance.

4.2.1 DC loss (copper loss)

Transmission lines are usually very thin tracks to comply with the characteristic impedance. This means, that the copper resistance is not negligible anymore when the traces become longer and parallel termination becomes low Ohmic.

The copper resistance is:

$$R_L = \rho \frac{L}{W \cdot t}$$

- $R_L$: resistance in mΩ
- $\rho$: specific resistance in Ωmm (0.0175 Ωmm for copper)
- $L$: trace length in mm
- $W$: trace width in mm
- $t$: trace thickness in mm

4.2.2 AC loss (skin effect)

The AC loss consists of multiple effects and is the conductor loss that is frequency dependent. When the frequency increases, the AC loss increases.

The effects that cause the conductor resistance to increase with frequency are:
- skin effect;
- surface roughness;
- proximity effect.

Effectively the skin effect is the cause for the frequency dependent loss. The surface roughness and proximity effect will increase the influence of the skin effect and cause the AC loss to be even higher.
4.2.2.1 Skin Effect

For DC the current distribution through a conductor is uniform. However, for higher frequencies the current redistributes itself towards the surface of the conductor. This phenomenon is called the skin effect.

The cross section through which the high-frequency current will flow is called the skin depth. Higher frequencies yield less skin depth while increasing the loss.

![Figure 13: Skin effect in cross section of conductor](image)

4.2.2.2 Surface Roughness

At low frequencies the surface roughness of a trace has a negligible effect on the AC loss.

As frequencies get higher, the skin effect will force the current to the outside of the conductor towards the surface. When the surface of the conductor is rough, the distance the current has to travel increases thus the AC loss increases. The surface roughness may cause the skin effect to almost double for high frequencies.

![Figure 14: Surface roughness](image)

4.2.2.3 Proximity Effect

As a result of the magnetic fields caused by the current through the wire and the return path, the current through the conductor will not flow through the conductor in a uniform way. This effect is called the proximity effect.

![Figure 15: Proximity effect](image)
As described in the previous paragraph, the current will flow through the outer side of the conductor due to the skin effect. The skin effect will cause the resistance to increase with frequency. Current that tends to flow through the conductor near its return path is called the proximity effect. The proximity will increase the conductor resistance even more than the skin effect and the surface roughness together. Dependent on the PCB stack-up, the skin effect and surface roughness effect are increased with a factor of 1.5 to 2.

4.2.3 Total Conductor Loss

The total resistive loss is determined by the DC loss and AC loss calculations. Since the AC loss is frequency dependent, the total loss will be frequency dependent.

At low frequencies the AC loss will be small and the total loss will be mainly determined by the DC loss. At higher frequencies the conductor loss will be mainly determined by the AC loss and the DC loss will be negligible.

4.3 Dielectric Loss

Dielectric loss is the loss introduced by the isolating material between two conductors. The dielectric loss is frequency dependent and causes the higher frequencies to be attenuated more than lower frequencies.

The attenuation caused by the dielectric loss becomes very large as frequencies become higher. Above around 2GHz the dielectric loss becomes higher than the conductor loss. There are many dielectric materials available which have a much better high frequency performance than the commonly used FR4 material. Main drawback is that these high-frequency materials are more costly and not every supplier uses the same type of high-frequency materials. For this reason, unless there is a specific need to use high-frequency dielectrics, standard FR4 is used taking these properties into account.

There are many dielectric materials available with two main properties, the dielectric constant and loss tangent. Both the dielectric constant and the loss tangent determine the dielectric loss of the signal.

4.4 Total Loss

The total loss signals are experiencing on a PCB interconnect is the conductor loss and dielectric loss together.

The maximum allowable total loss can be determined from the specified transmitter output levels and receiver input levels. In many standards (such as PCI Express) the maximum allowable attenuation for a portion of the interconnect is specified.

Many precautions can be taken to keep the attenuation within acceptable limits. The dielectric loss can be kept to a minimum when using the PCB outer layers or, when no other options exist, use different dielectric material. The conductor loss can be kept to a minimum by correct dimensioning of the trace width and PCB stack-up.
5. Crosstalk

Crosstalk is the disturbance on a trace due to a level transition on other traces as a result of the electric and magnetic field created by the transition.

Crosstalk is caused by the capacitive and inductive coupling between two traces. The level transition creates an electric field that is coupled into the victim trace via a mutual capacitance; the magnetic field is coupled by the mutual inductance between the traces.

Crosstalk is dependent on three main parameters:
- distance; distance between the aggressor and victim trace;
- length; the length of the aggressor and victim trace routed parallel;
- rise and fall times, signal speed transmitted over the aggressor trace.

Crosstalk between aggressor and victim trace can be reduced by varying one or more of these three parameters. Increasing the distance, decreasing the length and/or decreasing the rise and fall times of the signal will all reduce the crosstalk effect. When the distance between aggressor and victim is doubled, the crosstalk effect is reduced squared, so reduced by a factor four.

Differential signals (used for high speed serial interfaces) are less susceptible to crosstalk than single ended traces. With differential signals the voltage differences between the two conductors represent the signal amplitude. In an ideal situation both signal lines of the differential pair are disturbed by the same noise level, they will be subtracted from each other by the receiver and have no effect. In practice, one trace of the differential pair is closer to the aggressor than the other causing a difference in level of disturbance. Rule of thumb is that the distance between two differential pairs is 5 times the width of the trace or the distance between the traces, whichever is largest.

On today’s high-density PCBs every signal trace (victim) has many aggressors. It is not easy to calculate the effect of crosstalk due to many dependencies such
as PCB stack-up, direction of the transmitted signal, rise/fall time variations, etc. A board simulator (post-layout) helps to quantize the effect of all aggressors to the signal on the victim trace.
6. Timing

Signal integrity is not only depending on the quality of the waveform, but also on the timeliness of the signals arriving at the inputs of the chip.

6.1 Propagation delay

The propagation time is the time the signal requires to travel over a transmission line from driver to receiver. The propagation time is important for:

- a parallel bus, a clock signal is used to clock the parallel transmitted data into the receiver;
- high-speed (serial) signals, where the higher frequency components of the signal have a different propagation velocity.

The propagation time (or propagation velocity) can be calculated with the following formula.

\[ V_p = \frac{C}{\sqrt{\varepsilon_r}} \]

Where:
- \( V_p \) = Propagation velocity
- \( C \) = Speed of light (299,792,458 m/s)
- \( \varepsilon_r \) = Relative dielectric constant

The effective dielectric constant for traces on the outer layers differs from the inner layers, this causes the propagation velocity to be different. Special care has to be given to signals of a parallel bus (matching line length) which are routed on different layers (inner and outer layers).

For standard FR4 material the \( \varepsilon_r \) is different in frequency dependency. The higher the frequency, the lower the \( \varepsilon_r \). The difference in \( \varepsilon_r \) causes the high frequency signals to propagate faster over a trace than low frequency signals. Especially for serial interfaces this effect should be considered since transmitted data has different ‘frequencies’ in the transmitted data pattern.

6.1.1 Parallel busses

Synchronous parallel busses consist of clock, data, address and some control signals. All of these signals are clocked into the receiver by the clock signal and must arrive at a specified time with respect to the clock signal (setup & hold time). When the difference in propagation delay between clock and other signals becomes too high, this will result in errors. Therefore, the propagation delay difference (skew) between the signals should be kept between limits to guarantee error free transmission.

6.1.2 Serial Interfaces

For serial interfaces there is no separate clock distributed next to the data signal. Instead, the clock is extracted from the data pattern. The data pattern is encoded to guarantee a minimum number of bit transitions and allow the receiver to recover a clock from the data. Internal to the receiver the recovered clock is used to determine if a bit is a one or a zero in the middle of the period of the recovered clock. Performance of serial interfaces either by simulation or by measurements can be presented with so called ‘eye diagrams’. Many transitions are stacked on top of each other and show the quality of the signal. There should be a sufficiently clean open eye for the signal to have a low Bit Error Rate (BER)
High-speed serial interfaces use differential pairs for interconnect. When the lengths of the two traces in a differential pair differ (due to bends, changing layers and/or connections to devices), this will cause a distortion in the eye opening. Rule of thumb is to minimize the skew between the traces of a differential pair to 20% of the rise time. For a 10Gbps signal the maximum length difference between the traces is around 1mm!

6.2 Jitter

What is jitter?

Jitter is short-term variation of the significant instants of a digital signal from their ideal positions in time. In other words, jitter is interference in the time domain. Jitter will result in a signal with degraded eye opening (time as well as amplitude). Jitter is unwanted since it can cause a faulty detection of a bit level.

In Figure 18 jitter is represented for a data signal. The TIE (Time Interval Error) is the time between the actual edge of the data signal and the time the edge was expected. The TIE can be positive or negative. When the TIE is recorded for a longer time the difference between the maximum and minimum recorded TIE is called (peak-to-peak) jitter over the measured period of time. Figure 19 represents an eye diagram of a data signal with a certain amount of jitter.

Jitter can be divided in two categories: bounded (also called deterministic) and unbounded (random) jitter. Total jitter is the combination of both bounded and
unbounded jitter. Bounded jitter is the jitter that will not grow with time. Unbounded jitter will grow with time and has a Gaussian distribution.

Both deterministic and random jitter may have different sources. These jitter sources (such as supply ripple, oscillator jitter, etc.) have to be considered in the design phase and minimized to guarantee error free transmission.
7. RAIL & Ground bounce

In many publications the noise in response to drivers switching is described as ground bounce. However, a similar effect is incurred on the supply voltage. In most cases the supply voltage fluctuations are of less interest compared to the ground bounce effect since all signals are referenced to ground and not to the supply voltage.

Rail & ground bounce are a result of momentary currents introduced by switching levels in a driver circuit.

![Figure 20: Momentary current as a result of switching levels](image)

The output capacitance and the capacitance of the inputs connected with this output need to be loaded and unloaded when switching levels. The loading and unloading currents result in momentary currents.

![Figure 21: Loading and unloading of the internal output capacitor](image)

Ground and supply bounce voltage variations are caused by the momentary currents in the inductance of the power and ground connections. The inductance is a combination of the package internal inductance (bounding wires and internal connections) and induction of the power and ground connections (planes or traces) on the PCB.

The influence of PCB trace and plane induction can be reduced by placing decoupling capacitors as close to the package pins as possible. The package internal induction on power and ground connections however cannot be compensated for and will give a distortion on the signal due to the momentary currents caused by switching levels. When one output switches its level other outputs with a common ground and power will also suffer from the voltage variation on the power and ground rail.
When multiple outputs switch levels at the same moment, these momentary currents will add up and cause even larger voltage variations. Devices with a large number of IO pins (such as FPGAs) often have a SSO (Simultaneous Switching Outputs) limit per power and ground group. The SSO parameter describes how many outputs may switch at the same time and keep the voltage variations to acceptable levels and guarantee correct functioning.
8. High Speed Design

Designing high speed printed circuit boards is an inherently complex matter. Many of the effects are frequency dependent and interact with each other. Without taking these phenomena into account the reliability of the board cannot be guaranteed.

Simulation is used to predict and find the bottlenecks in designs but will not solve them. Simulations are based on simulation models that are provided by the component vendors and come in different flavors and are varying in accuracy. A common type of simulation model is an IBIS model. IBIS models are relatively simple (to allow fast simulation) but have a few shortcomings. We are able to convert the IBIS models to more accurate Spice models.

A high-speed designer needs to know all of the described phenomena and their effect to be able to create a high frequency reliable board first time right. Patching a prototype board at these frequencies will be impossible from both physical and electrical point of view.

Measurements will be performed on the board to verify the calculated and simulated effects. When comparing measurement results with simulation results at real high frequencies it is even necessary to include the model of the measurement probes into the simulation for a realistic comparison.

The design verification measurements are performed on prototype boards. Correct functioning of many manufactured boards can only be guaranteed when component and production process variations are taken into account during the design phase.