Hardware Design Language (HDL)
About Technolution and me

- **Technolution**
  - Developer and supplier of working systems and products

- **Gideon Zweijtzer**
  - System Architect
  - Expertise: electronics & programmable logic
Introduction

- We develop products
- We have adopted an agile way of working
- This presentation focuses on electronics design

- What can we do to get better results in less time?
Design Flow

• From concept to implementation to product

• We build systems, not just boards

• Complexity is increasing

• Many aspects to be considered
  • Results in many ‘views’
  • Each ‘view’ explained in a simple diagram
Observations

• What is the true purpose of a schematic drawing?
• A schematic contains lots of details
• Synchronizing schematics and documents is difficult
• A schematic is used to create a netlist for digital parts
• Trend is to store designs in binary format
Wish list

- Single source of design information
- Design contains only relevant component parameters
- Open format
- Version control
Paradigm shift
Paradigm shift

We no longer *draw* schematics
We type!

We have developed a domain-specific language
 together with a compiler
New design flow
HDL features

- HDL describes signal paths $\rightarrow$ compact and readable
- HDL contains the design information required for component selection

\[
gpio[5] \Rightarrow R(220 \text{ Ohm, power } \geq 100\text{mW}) \Rightarrow \\
\text{smd\_led(color = 'green') <cathode; anode> } \Rightarrow v33;
\]

- Expression evaluation for in-module calculations
  - Series resistors, filter capacitances,
  - Voltage feedback resistor dividers,
  - …
Example

\[
i_{ddr} : \text{MT46H32M32LFCM}() < \\
\text{test} \Rightarrow \text{gnd};
\]

\[
i_{imx} : \text{MCIMX35}() < \\
\text{sdclk} \Rightarrow \text{R(33)} \Rightarrow \text{ddr.ck} \Rightarrow \text{decap(1.8p)};
\]

\[
\text{sdcke[0]} \Rightarrow \text{ddr.cke};
\]

\[
\text{sdcke[1]} \Rightarrow \text{open};
\]

\[
\text{a[9:0]} \Rightarrow \text{ddr.a[9:0]};
\]

\[
\text{ma10} \Rightarrow \text{ddr.a[10]};
\]

\[
\text{a[12:11]} \Rightarrow \text{ddr.a[12:11]};
\]

\[
\text{sdba} \Rightarrow \text{ddr.ba};
\]

\[
\text{cs_n[2]} \Rightarrow \text{ddr.cs_n};
\]

\[
\text{sdras_n} \Rightarrow \text{ddr.ras_n};
\]

\[
\text{sdcas_n} \Rightarrow \text{ddr.cas_n};
\]

\[
\text{sdwe_n} \Rightarrow \text{ddr.we_n};
\]

\[
\text{dqm} \Rightarrow \text{ddr.dm};
\]

\[
\text{dqs[3:0]} \Rightarrow \text{R(33)} \Rightarrow \text{ddr.dqs} \Rightarrow \text{decap(1.8p)};
\]

\[
\text{sd} \Rightarrow \text{ddr.dq};
\]
module parameterization

module amplifier(gain = 2.5)
{
    interface {
        ...
    }
    R2 = 100 kOhm;
    R1 = \texttt{E24}(R2 / (gain - 1));

    my_amp : opamp() <-
        pos  => input;
        out  => output  => R(R2)  => my_amp.neg;
        neg  => R(R1)  => GND;
        vplus => Vplus;
        vmin  => Vmin;
    >;
}

This module implements a simple non-inverting amplifier, using an operational amplifier (opamp). The opamp chosen is the '$(opamp.order_code)' from '$(opamp.manufacturer)'.

Gain = 1 + (R2/R1), thus when R2 is given, R1 can be calculated as: R2 / (gain - 1). The requested gain is $(gain). R2 is chosen to be $(R2). Therefore, R1 should be $(R1).
Best of both worlds

- A schematic drawing is useful for some classes of circuits
- HDL compiler supports reading schematic sheets
  - Conversion to HDL internally
- HDL compiler ‘links’ the imported sheets with the other code
Additional benefits

- Automatic checking and verification
  - Circuit consistency
  - Logic level verification
  - Pull-ups, strapping
- Automatic calculations; power, MTBF, …
- Embed layout constraints

*More and better results in less time!*
Experiences with HDL

- Learning curve
- Designers easily adapt to using HDL
- Introducing HDL: developing new reflexes / patterns
- In process of developing a HDL programming style
- Roadmap
Summary

- Technolution innovates
  - Also on design methods!

- Describing electronics using text is a success
  - Follows the success of software and FPGA development

- HDL helps to reduce cost and/or time-to-market
- HDL is a valuable addition to our tool box
- We are interested in developing HDL further with other vendors

- Visit stand 37 for more information / demo!
Questions?
Visit us at stand 37